IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 1, 3 and 7-9 and AMEND claims 2 and 4 in accordance with the following:

1. (Cancelled)

2. (Currently Amended) A device for transmitting a wired OR signal between two systems, each system comprising:

output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line, and outputting either state to the other system;

switching control means for switching an output state of said output means; and

an assert mechanism that maintains the wired OR signal line in an asserted state in response to an asserted state transferred by the output means of the other system;

~~The device for transmitting a wired OR signal between two systems according to claim 1,~~ wherein said switching control means comprises a register controlled by a processor in the system, and said output means comprises:

a mask mechanism which switches to said first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value; and

a transmission mechanism that transfers an output from said mask mechanism to the other system.

3. (Cancelled)

4. (Currently Amended) A device for transmitting a wired OR signal between two systems, each system comprising:

output means for outputting the signal state of a wired OR signal line to the other system;

switching and outputting means for switching between the first state where the signal

state transmitted by the output means in the other system is output and the second state where negate state is output, and outputting the switched state;

switching and controlling means for switching the output of said switching and outputting means; and

an assert mechanism that switches the wired OR signal line between an asserted state or a negate state according to the output state of said switching and outputting means;

~~The device for a transmitting wired OR signal between two systems according to claim 3,~~ wherein said switching and controlling means is composed of a register controlled by a processor in the system, and said switching and outputting means is composed of a mask mechanism which switches to the first state when said register has a predetermined value and switches to the second state when the register has a value other than the predetermined value.

5. (Previously Presented) A method for communicating a wired OR signal between two systems, in which each system comprises output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the wired OR signal line, and outputting either state to the other system, and assert means for maintaining the wired OR signal line in the system in an asserted state in response to an assert signal from the output means of the other system, the method comprising:

switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state;

processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching; and

switching each of said output means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said output means to the first state.

6. (Previously Presented) A method for transmitting a wired OR signal between two systems, in which each system comprises output means for outputting the signal state of a wired OR signal line to the other system; switching and outputting means for switching between the first state where the signal state transmitted by the output means in the other system is output and the second state where negate state is output, and outputting the switched state; switching and controlling means for switching the output of said switching and outputting means; and an

assert mechanism that switches the wired OR signal line between an asserted state or a negate state according to the output state of said switching and outputting means; the method comprising:

switching the wired OR signal line in one of the two systems to the asserted state if the wired OR signal line of the other system is brought into the asserted state, when each of the switching and outputting means is in the first state;

processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching; and

switching each of said switching and outputting means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said switching and outputting means to the first state.

7-9. (Cancelled)